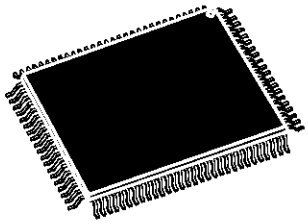
SGS-THOMSON MICROELECTRONICS

M63532P

32Kx32 PIPE-LINED BRAM LOW VOLTAGE CACHE BURST SRAM

PRELIMINARY DATA

- 32Kx32 SYNCHRONOUS SRAM
- LOW VOLTAGE: 3.3V ± 0.3V
- PIPE-LINED OUTPUT REGISTERS SUPPORTS 3-1-1-1 CACHE BURST LINE FILLS
- FAST CYCLE TIMES: 75, 66, 60MHz
- CLK to DATA ACCESS: 7, 8, 9ns Max
- INTERLEAVE or LINEAR BURST COUNTER
- INPUT & OUTPUT REGISTERS
- SELF-TIMED WRITE CYCLE
- THREE STATE COMMON I/O
- ASYNCHRONOUS OUTPUT ENABLE ($\overline{OE}$)
- BURST CONTROL INPUTS: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$
- BYTE WRITE SELECTS: ($\overline{BWE1}$ - $\overline{BWE4}$)
- GLOBAL WRITE ENABLE ($\overline{GW}$)
- JEDEC STANDARD 100 PIN TQFP
- SNOOZE MODE INPUT



TQFP100 (LT)
14 x 20mm

DESCRIPTION

The M63532P BRAM® is a 1,048,576-bit CMOS Burst SRAM, organized as 32,768 words x 32 bits. It is fabricated using SGS-THOMSON's low power, high performance, 3.3V HCMOS technology. The device integrates a 2-bit burst counter, address registers, input and output registers, and high speed synchronous SRAM onto a single chip. The M63532P is specifically adapted to provide a burstable, high performance secondary cache for fourth and fifth generation X86 and RISC microprocessors. The device has output registers to support pipe-lined read operations where output data is provided from the previous cycle at the rising edge of clock.

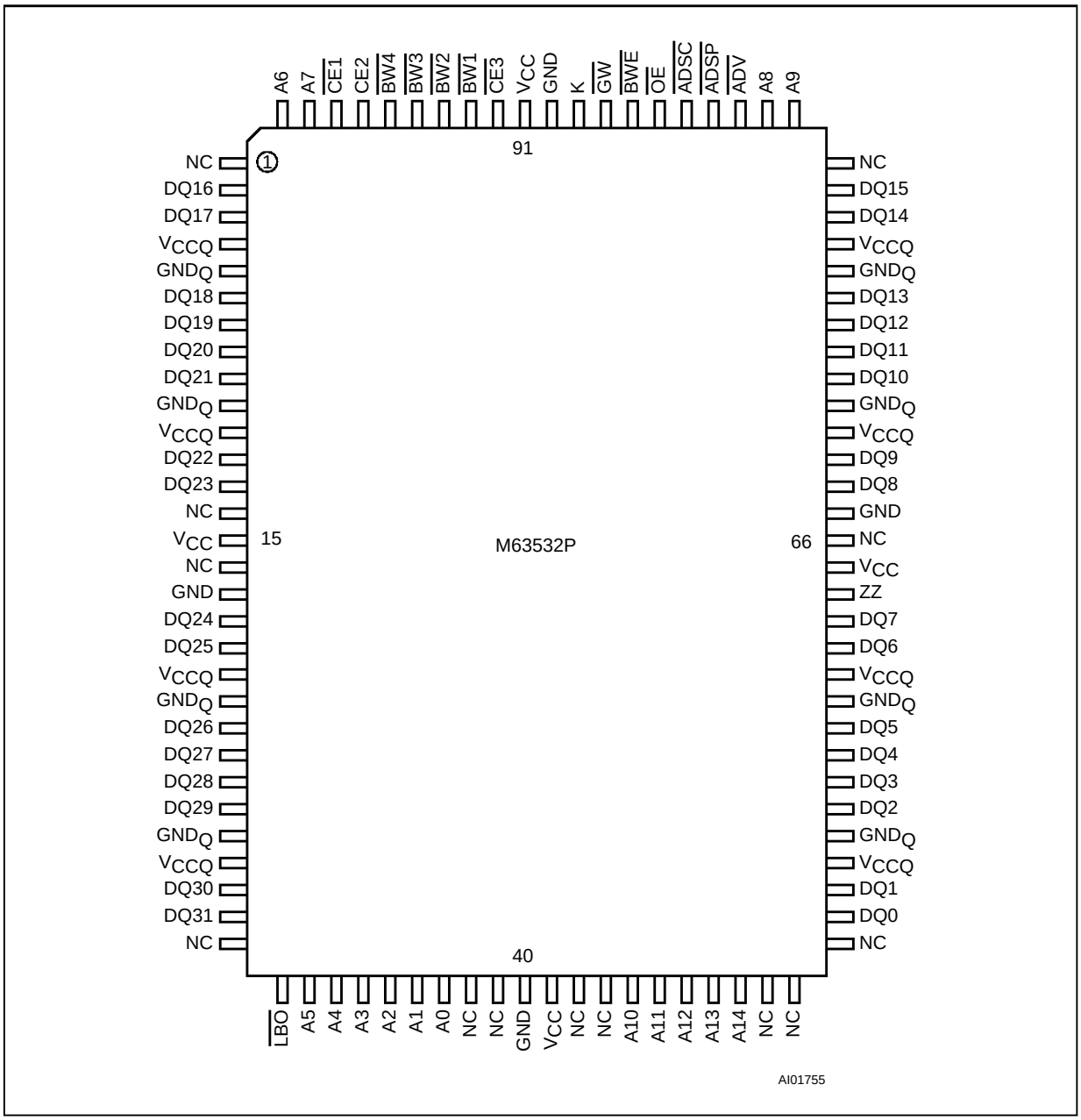
The M63532P is available in a 100 pin 14x20mm JEDEC standard thin quad plastic flat-pak (TQFP). The device provides multiple power and ground pins to reduce effects induced by output noise for high performance applications. All power (V_{CC} and V_{CCQ}) and ground (GND, and GND_Q) pins must be used for proper device operation. The BRAM requires a 3.3V± 0.3V power supply, and all inputs and outputs are TTL compatible.

Table 1. Signal Names

A0-A14	Address Inputs
DQ0-DQ31	Data Input/Output
K	Clock
$\overline{LBO}$	Linear Burst Order Select
$\overline{BWE}$	Byte Write Enable
$\overline{BW1}$-$\overline{BW4}$	Byte Write Selects
$\overline{GW}$	Global Write Enable
$\overline{OE}$	Output Enable
$\overline{CE1}$	Master Chip Enable
CE2	Active High Chip Select
$\overline{CE3}$	Active Low Chip Select
$\overline{ADSP}$	Address Status Processor
$\overline{ADSC}$	Address Status Controller
$\overline{ADV}$	Burst Address Advance
ZZ	Snooze Mode Input
V_{CC}	Supply Voltage (Core)
GND	Ground (Core)
V_{CCQ}	Supply Voltage (DQ)
GND_Q	Ground (DQ)

Note: All power and ground pins must be connected for proper device operation.

Figure 1. Pin Connections



Warning: NC = Not Connected.

DEVICE OPERATIONS

Burst operations can be initiated with either $\overline{ADSP}$ (processor address status) or $\overline{ADSC}$ (controller address status). The burst advance input $\overline{ADV}$, allows the next burst address to be generated internal to the BRAM.

Cache burst read cycles are initiated with $\overline{ADSP}$, without regard to $\overline{ADSC}$ or $\overline{BWE}$, using the external address clocked into the on-chip address registers when $\overline{ADSP}$ is sampled LOW. All Chip Selects must be asserted for $\overline{ADSP}$ to begin the burst cycle. The output buffers will be enabled by $\overline{OE}$ when the BRAM is selected. If the device is going from a deselect to a select mode, the device will be selected and the outputs enabled on the following clock cycle. In a read operation, data accessed by the current registered address will be available t_{KQ} from the next rising clock edge in a pipe-lined fashion.

Table 2. Pin Description

Signal	I/O	Property Asserted	Pin#	Description
K	I	CLOCK	89	Clock: All inputs except $\overline{OE}$ and ZZ are synchronous to the rising edge of K.
A0-A14	I	SYNC	Note 1	Address: Sampled when Chip Selects are true and $\overline{ADSP}$ or $\overline{ADSC}$ is asserted active LOW at the rising edge of K.
DQ0-DQ31	I/O	SYNC	Note 2	SRAM data Input/Outputs: DQs remain high impedance except when $\overline{OE}$ is asserted LOW. Data In is valid during write cycles, Data Out is valid during read cycles provided $\overline{OE}$ is asserted.
$\overline{CE1}$	I	SYNC, LOW	98	Master Chip Enable: Sampled on the rising edge of K with $\overline{ADSP}$ or $\overline{ADSC}$. When $\overline{CE1}$ is HIGH, $\overline{ADSP}$ is blocked. Refer to the synchronous truth table.
CE2	I	SYNC, HIGH	97	Synchronous Chip Select, used to select the device, and for memory depth expansion. Sampled when a new address is loaded.
$\overline{CE3}$	I	SYNC, LOW	92	Synchronous Chip Select, used to select the device, and for memory depth expansion. Sampled when a new address is loaded.
$\overline{ADSP}$	I	SYNC, LOW	84	Address Status Processor: Used to load a new address or select the device.
$\overline{ADSC}$	I	SYNC, LOW	85	Address Status Cache Controller: Used to load a new address, or select or deselect the device.
$\overline{ADV}$	I	SYNC, LOW	83	Burst Address Advance: Commands internal burst counter.
$\overline{GW}$	I	SYNC, LOW	88	Global Write Enable: Supersedes all other write enable inputs.
$\overline{BWE}$	I	SYNC, LOW	87	Master Byte Write Enable: Must be asserted with one or more byte select signals during a write cycle to perform a write operation to the SRAM.
$\overline{BW1}$-$\overline{BW4}$	I	SYNC, LOW	Note 3	Byte Write Selects to select 1 of 8 bit bytes of the 32-bit data bus.
$\overline{OE}$	I	ASYNC, LOW	86	Output Enable: Asynchronous DQ control when the device is selected.
$\overline{LBO}$	I	STATIC	31	Linear Burst Order: GND = Linear burst count. V_{CC} = Interleave burst count. The $\overline{LBO}$ input must be tied to V_{CC} or GND, and cannot change during device operation.
ZZ	I	ASYNC, HIGH	64	Snooze Mode Input: Overrides all control logic. Requires all inputs at CMOS levels. Asserted HIGH. The ZZ pin is tied to GND if this mode is not used. (See ZZ Mode table and timing.)
V_{CC}	Supply	3.3V	Note 4	Core Power Supply: 3.3V ± 0.3
GND	Supply	Ground	Note 5	Device ground: 0 volts.
V_{CCQ}	Supply	3.3V	Note 6	Isolated Output Buffer Supply: 3.3V ± 0.3
GND_Q	Supply	Ground	Note 7	Isolated Output Buffer Ground: 0 volts.

Notes: 1. Address inputs are listed respectively as A0-A14: 37,36,35,34,33,32,100,99,82,81,44,45,46,47,48.
2. DQs are listed respectively as D0-D31: 52,53,56,57,58,59,62,63,68,69,72,73,74,75,78,79,2,3,6,7,8,9,12,13,18,19,22,23,24, 25,28,29.
3. Byte Write Selects are listed respectively as: $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$: 93,94,95,96
4. V_{CC} pins: 15,41,65,91
5. GND pins: 17,40,67,90
6. V_{CCQ} pins: 4,11,20,27,54,61,70,77
7. GND_Q pins: 5,10,21,26,55,60,71,76

Figure 2. Block Diagram

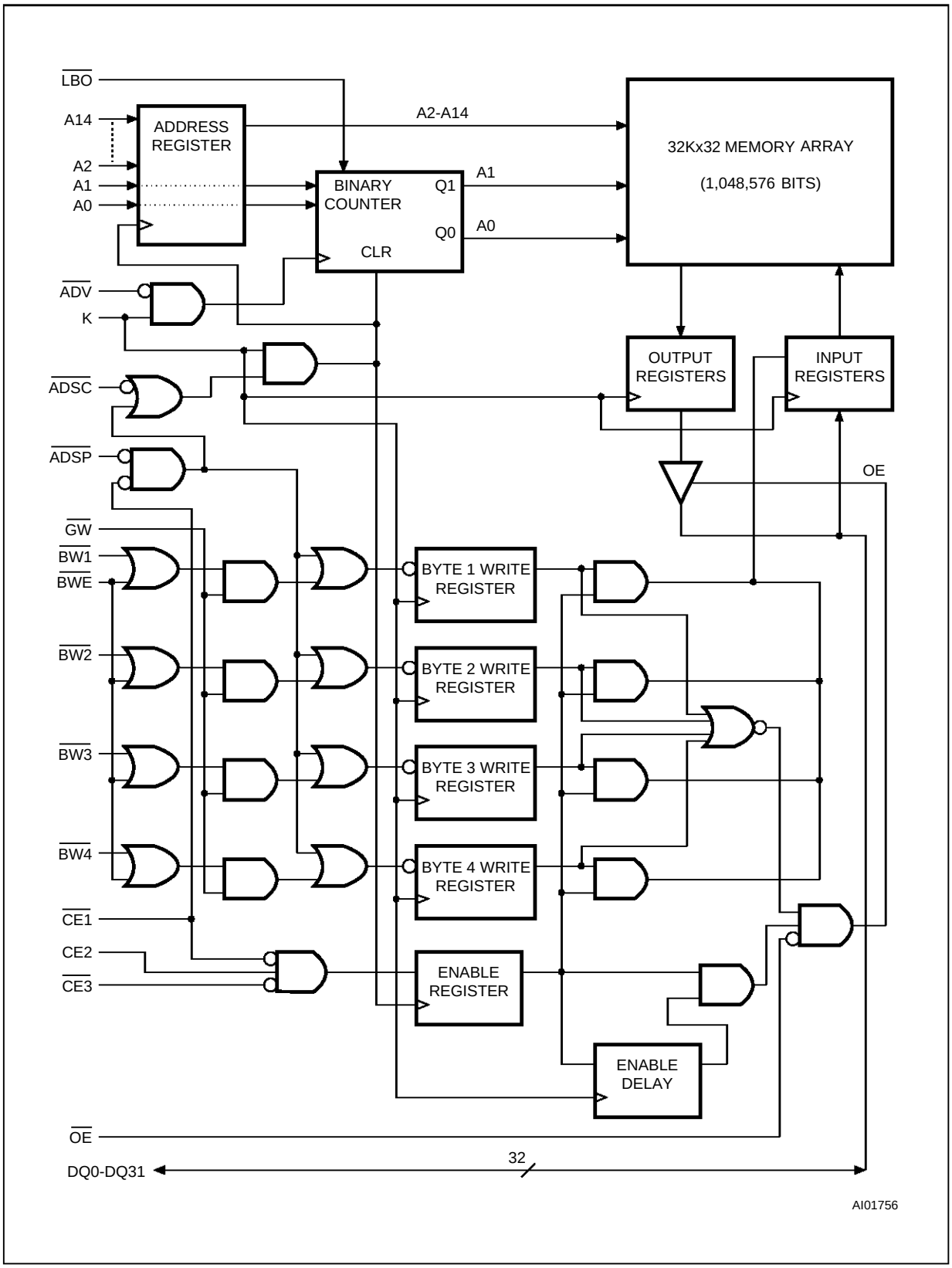


Table 3. Synchronous Truth Table

No.	$\overline{CE1}$	$\overline{CE3}$	CE2	$\overline{ADSP}$	ADSC	ADV	$\overline{WE}$	$\overline{OE}$	K	DQ	Address	Operation
1	H	X	X	X	L	X	X	X	↑	Hi-Z	None	Deselect, Power-down
2	L	X	L	L	X	X	X	X	↑	Hi-Z	None	Deselect, Power-down
3	L	H	X	L	X	X	X	X	↑	Hi-Z	None	Deselect, Power-down
4	L	X	L	H	L	X	X	X	↑	Hi-Z	None	Deselect, Power-down
5	L	H	X	H	L	X	X	X	↑	Hi-Z	None	Deselect, Power-down
6	L	L	H	L	X	X	X	L	↑	Q	External	Read Cycle Begin Burst
7	L	L	H	L	X	X	X	H	↑	Hi-Z	External	Read Cycle Begin Burst
8	L	L	H	H	L	X	L	X	↑	D	External	Write Cycle Begin Burst
9	L	L	H	H	L	X	H	L	↑	Q	External	Read Cycle Begin Burst
10	L	L	H	H	L	X	H	H	↑	Hi-Z	External	Read Cycle Begin Burst
11	X	X	X	H	H	L	H	L	↑	Q	Next	Read Cycle Continue Burst
12	X	X	X	H	H	L	H	H	↑	Hi-Z	Next	Read Cycle Continue Burst
13	H	X	X	X	H	L	H	L	↑	Q	Next	Read Cycle Continue Burst
14	H	X	X	X	H	L	H	H	↑	Hi-Z	Next	Read Cycle Continue Burst
15	X	X	X	H	H	L	L	X	↑	D	Next	Write Cycle Continue Burst
16	H	X	X	X	H	L	L	X	↑	D	Next	Write Cycle Continue Burst
17	X	X	X	H	H	H	H	L	↑	Q	Current	Read Cycle Suspend Burst
18	X	X	X	H	H	H	H	H	↑	Hi-Z	Current	Read Cycle Suspend Burst
19	H	X	X	X	H	H	H	L	↑	Q	Current	Read Cycle Suspend Burst
20	H	X	X	X	H	H	H	H	↑	Hi-Z	Current	Read Cycle Suspend Burst
21	X	X	X	H	H	H	L	X	↑	D	Current	Write Cycle Suspend Burst
22	H	X	X	X	H	H	L	X	↑	D	Current	Write Cycle Suspend Burst

Notes: 1. X = Don't Care. H is logic HIGH. L is logic LOW. The ZZ input is presumed LOW for all cases of the truth table.
2. This is a synchronous device. All inputs except $\overline{OE}$ must meet the specified setup and hold times relative to the rising edge of K.
3. $\overline{ADSP}$ = LOW at the rising edge of K initiates an internal Read operation when the device selected. ($\overline{ADSP}$ can be blocked if $\overline{CE1}$ is HIGH). A Write operation can only be performed on the subsequent clock.
4. $\overline{WE}$ = L means a valid write cycle is initiated by proper assertion of write enable signals. A Write cycle is defined by at least one Byte Write (BW4-BW1) asserted with $\overline{BWE}$, and $\overline{ADSP}$ HIGH for the specified set-up and hold times.
5. READ cycles are defined by all Write Enables held HIGH for the specified set-up and hold times relative to the rising edge of K.
6. For a Write operation following a Read operation, $\overline{OE}$ must be HIGH t_{OEHZ} before the input data required setup time and held HIGH throughout the input data hold time.
7. This device contains circuitry that ensures the DQs will be High-Z during power-up.
8. $\overline{OE}$ controls the state of the data bus (DQ) when the device is selected. DQs are High-Z when the device is deselected. $\overline{OE}$ is a "don't care" when a byte write enable is sampled low initiating a valid Write cycle.
9. The device is presumed selected in a previous cycle for logic states 11-22.

Table 4. ZZ Mode Truth Table

ZZ	$\overline{CE1}$	$\overline{CE3}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{GW}$	$\overline{OE}$	K	DQ	Address	Operation
H (1)	X	X	X	X	X	X	X	X	X	X	X	Sleep Mode
L	Valid	Valid	Valid	Valid	Valid	Valid	Valid	Valid	Valid	Valid	Valid	See Synchronous Table (2)

Notes: 1. When ZZ is asserted HIGH, the device will enter a Snooze Mode within t_{ZZS}. K must continue for a minimum of two valid cycles once ZZ goes HIGH.
2. Refer to the Synchronous Truth Table given above.

Table 5. Partial Write Truth Table

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$	DQ Control
Read	H	H	X	X	X	X	Q0-Q31
Read	H	L	H	H	H	H	Q0-Q31
Write Byte1	H	L	L	H	H	H	D0-D7
Write Byte2	H	L	H	L	H	H	D8-D15
Write Byte3	H	L	H	H	L	H	D16-D23
Write Byte4	H	L	H	H	H	L	D24-D31
Write All Bytes	H	L	L	L	L	L	D0-D31
Write All Bytes	L	X	X	X	X	X	D0-D31

Notes: 1. X = Don't Care. H is logic HIGH. L is logic LOW.
2. All byte write signals are synchronous inputs to the rising edge (LOW-to-HIGH) transition of K.

DEVICE OPERATIONS (cont'd)

The $\overline{ADV}$ input is ignored on the clock edge that samples $\overline{ADSx}$ asserted, but is sampled on all subsequent clock edges. The address is incremented internally to the BRAM for each read burst access where $\overline{BWE}$ and $\overline{GW}$ are sampled HIGH, $\overline{ADV}$ is asserted LOW, and both address strobes are HIGH. Data is always valid at t_{KQ} for all Outputs (DQ0-DQ31) from the rising of clock (K).

The $\overline{ADV}$ input (burst address advance) provides control of the burst counter. The $\overline{ADV}$ input controls subsequent burst data accesses after the first data of the burst cycle is processed. Each time $\overline{ADV}$ is active low for subsequent bursts at the rising edge of the clock input, the burst counter is advanced to the next burst address. The address is advanced before the operation. The BRAM will suspend the address burst sequence when the $\overline{ADV}$ pin is high during positive clock transitions. Upon completion of the full internal burst count, the address will wrap-around to its initial base address. The logic state of the $\overline{LBO}$ input determines the burst sequence as interleave (i486™ or Pentium™ for Intel bursts) or linear for other processors (RISC, Power PC, Cyrix 6x86).

Write cycles are performed by disabling the outputs with $\overline{OE}$ prior to asserting $\overline{BWE}$.

A global write enable ($\overline{GW}$ = LOW) writes all 32 bits regardless of the state of $\overline{BWE}$ or individual byte write select inputs. When $\overline{GW}$ is HIGH, one or more bytes can be written by asserting $\overline{BWE}$ and individual byte write selects ($\overline{BWE1}$ - $\overline{BWE4}$). The byte write table shows which byte write selects controls DQ0-DQ31. $\overline{BWE}$ is ignored on rising clock edges that sample $\overline{ADSP}$ LOW, but is sampled on all subsequent rising clock edges.

Output buffers are disabled t_{KQHZ} after K when $\overline{BWE}$ or $\overline{GW}$ is sampled LOW (independent of $\overline{OE}$). Data is clocked into the data input register when a proper write operation is implemented. The write cycles are internally self-timed, and are initiated by the rising edge of the clock input. A write burst cycle continues with the address incremented internal to the BRAM when $\overline{BWE}$ and $\overline{ADV}$ are sampled LOW at the next rising clock edge.

Table 6. Asynchronous Truth Table

Operation	$\overline{OE}$	DQ Status
Read	L	Data Out
Read	H	High-Z
Write (2)	X	Data In (High-Z)
Deselected (3)	X	High-Z

Notes: 1. X = Don't Care. H is logic HIGH. L is logic LOW.
2. For a cache write cycle following a read operation, $\overline{OE}$ must be high t_{OEHZ} before the input data required set-up time, and be held high through the input data hold time.
3. Deselect from previous cycle.

Table 7. Interleave Burst Sequence (LBO = V_{CC})

Burst Starting Address		Begin 1		Begin 2		Begin 3		Begin 4	
		A1	A0	A1	A0	A1	A0	A1	A0
Load External Address	A14-A2	0	0	0	1	1	0	1	1
1st Burst Address (Internal)	A14-A2	0	1	0	0	1	1	1	0
2nd Burst Address (Internal)	A14-A2	1	0	1	1	0	0	0	1
3rd Burst Address (Internal)	A14-A2	1	1	1	0	0	1	0	0

Note: The burst count sequence wraps around to the initial address after a full count is completed.

Table 8. Linear Burst Sequence (LBO = GND)

Burst Starting Address		Begin 1		Begin 2		Begin 3		Begin 4	
		A1	A0	A1	A0	A1	A0	A1	A0
Load External Address	A14-A2	0	0	0	1	1	0	1	1
1st Burst Address (Internal)	A14-A2	0	1	1	0	1	1	0	0
2nd Burst Address (Internal)	A14-A2	1	0	1	1	0	0	0	1
3rd Burst Address (Internal)	A14-A2	1	1	0	0	0	1	1	0

Note: The burst count sequence wraps around to the initial address after a full count is completed.

Read or Write operations can be initiated with $\overline{ADSC}$ instead of $\overline{ADSP}$. The differences of these inputs are noted as:

1.$\overline{ADSP}$ must be HIGH when $\overline{ADSC}$ is asserted LOW to initiate a cycle with $\overline{ADSC}$.

2.All Write Enable signals are sampled on the positive going clock edge that samples $\overline{ADSC}$ LOW (with $\overline{ADSP}$ HIGH).

3.$\overline{ADSP}$ is blocked when $\overline{CE1}$ is HIGH. The M63532P can be selected with either $\overline{ADSP}$ or $\overline{ADSC}$, but can only be deselected with $\overline{ADSC}$ when $\overline{CE1}$ is HIGH.

GENERAL APPLICATION

The M63532P provides an architecture for building a 32Kx64-bit burstable L2 data cache SRAM array (256K bytes) by using only two (2) devices. Four (4) devices are needed to provide a 512K byte cache (see Figure 9 and Figure 10). The M63532P BRAM has three chip enables for easy depth expansion. The chip enables are registered to allow contention free operation when implementing a 512K byte, dual-bank cache configuration.

Table 9. Write Pass-Thru Truth Table

Previous Cycle (x) [1]		Present Cycle (y)				Next Cycle (z)
Operation	$\overline{BWn}$ [4,5]	Operation	$\overline{CE}$ [2]	$\overline{BWn}$	$\overline{OE}$	Operation
Initiate WRITE cycle for ALL bytes Address = A(x); Data = D(x)	ALL Low	Initiate READ cycle, Register A(y), Q=D(x)	L	H	L	READ Q(y) [3]
Initiate WRITE cycle for ALL bytes Address = A(x); Data = D(x)	ALL Low	READ / DESELECT No new cycle Q=D(x)	H	H	L	No carry over from previous cycle (Deselect)
Initiate WRITE cycle for ALL bytes Address = A(x); Data = D(x)	ALL Low	READ / DESELECT No new cycle Q=High-Z	H	H	H	No carry over from previous cycle (Deselect)
Initiate WRITE cycle, one byte Address = A(x); Data = D(x)	One Low	READ / DESELECT No new cycle Q=D(x) for one byte	H	H	L	No carry over from previous cycle (Deselect)

Notes: 1. Previous cycle (x) can be either Burst or Non-burst.
2. $\overline{CE}$ = L means all Chip Enable inputs are True. $\overline{CE}$ = H means one or more Chip Enable inputs are False such that the device is deselected.
3. Write data Pass-Thru will occur when a Read cycle at address (y) is preceded by a Write cycle at address (x). Address (y) will be registered as the new address, and data written at address (x) will appear on the outputs (DQ) during the same clock period. The subsequent read cycle (z) will provide data from address (y) to the DQ pins. The $\overline{OE}$ input will maintain control of the data bus at all times.
4. $\overline{BWE}$ is LOW when one or more $\overline{BWn}$ inputs are LOW.
5. $\overline{GW}$ = LOW also writes all bytes giving identical results.

Table 10. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Voltage on any Pin Relative to Ground [1, 3]	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage [1, 2]	–0.5 to +4.6	V
I_O	Output Current [4]	100	mA
P_D	Power Dissipation	2	W

Notes: 1. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.
2. Accelerated life tests are performed with V_{CC} = 4.2 at 125°C
3. All pins except the V_{CC} pin. DC conditions only where V_{CC} for this parameter refers to the specified operating range of V_{CC}, where V_{CC} max. is 3.6 volts.
4. Output current absolute maximum rating is specified for one output at a time, not to exceed a duration of 1 second.

Table 11. Recommended DC Operating Conditions (1,2) (T_A = 0 to 70 °C)

Symbol	Parameter	Min	Typ.	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH} (3,5)	Logic '1' Input Voltage	2.0	3.0	V_{CC} + 0.3	V
V_{IHK} (3)	Logic '1' Clock only	2.0	3.0	5.5	V
V_{IHZZ} (3)	Logic '1' ZZ Input	2.4	3.0	V_{CC} + 0.3	V
V_{IL} (4,5)	Logic '0' All Inputs	–0.3	0.2	0.8	V
V_{CCQ}	Supply Voltage	V_{CC}	3.3	V_{CC}	V
GND_Q	Supply Voltage	0	0	0	V

Notes: 1. All voltages referenced to GND.
2. Minimum DC input levels are guaranteed at cycle times of 500ns.
3. V_{IH} max. = (V_{CC} + 1.0) AC (pulse width ≤ tKC/2). Input current limit 200mA.
4. V_{IL} min. = -1.0V AC (pulse width ≤ tKC/2). Input current limit 200mA.
5. The $\overline{LBO}$ pin is a CMOS static input and must be tied to either V_{CC} or GND for proper operation.

Table 12. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit
I_{CCA} (1)	Average AC Power Supply Current, device selected, ($\overline{OE}$=V_{IH}). All inputs = V_{IL} = 0.0V and V_{IH} ≥ 3.0V V_{CC} max., K cycle time = t_{KC} min.		290	mA
I_{CC1}	Device selected, ($\overline{OE}$=V_{IH}). $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$. $\overline{BWE}$, $\overline{GW}$, $\overline{BWn}$ ≥ V_{IH} ; all inputs ≤ (GND + 0.2) or ≥ (V_{CC} -0.2)no toggle; V_{CC} max., K cycle time = t_{KC} min. Read suspend.		50	mA
I_{SB2}	TTL Standby Current, device deselected, All inputs are static: ≤ V_{IL} or ≥ V_{IH} ; V_{CC} max., K cycle time = 0.		18	mA
I_{SB3}	CMOS Standby Current, device deselected, All inputs are static: ≤ (GND + 0.2) or ≥ (V_{CC} – 0.2) ; V_{CC} max., K cycle time = 0.		5	mA
I_{SB4}	Device deselected, All inputs are static: ≤ (GND + 0.2) or ≥ (V_{CC} – 0.2) ; V_{CC} max., K cycle time = t_{KC} min.		50	mA
I_{LI} (2)	Input Leakage Current (Any Input)	–2	2	µA
I_{LO} (2)	Output Leakage Current	–2	2	µA
V_{OH} (3)	Output Logic '1' Voltage (I_{OH} = -4.0mA)	2.4		V
V_{OL} (3)	Output Logic '0' Voltage (I_{OL} = 8mA)		0.4	V

Notes: 1. I_{CCA} measured as average AC current, with outputs open, V_{CC} max., t_{KC} (min) cycle 100%. All addresses are registered every other cycle.
2. Measured with $GND_Q \le V \le V_{CC}$ and outputs deselected.
3. All voltages referenced to GND_Q.

Table 13. Capacitance (1) (T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Typ	Max	Units
C_I	Input Capacitance on all pins (except DQ)	5	7	pF
C_O (2)	Output Capacitance (DQ0-DQ31)	6	8	pF

Notes: 1. Capacitances are sampled and not 100% tested.
2. Output buffers are deselected.

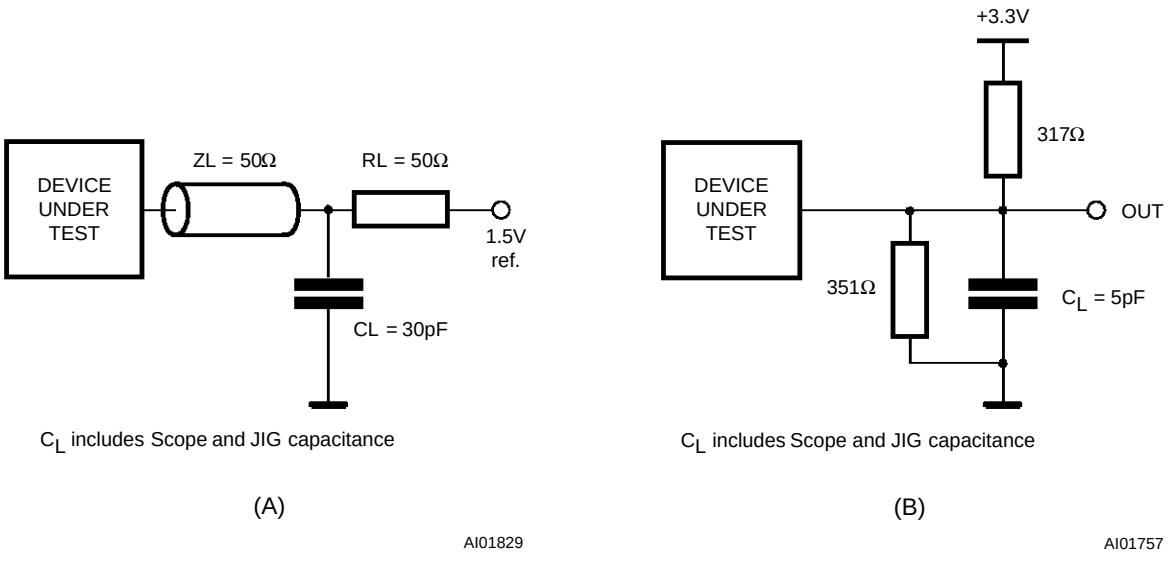
Table 14. Termal Consideration

Symbol	Description	Conditions	Typ	Units
Θ_{JA}	Thermal resistance, Junction to Ambient	Still Air, soldered onto a 4.34 x 1.13 inch, 8 layer, Printed Circuit Board	31	°C/ W
Θ_{JC}	Thermal resistance, Junction to Case		TBD	°C/ W

Table 15. AC Test Condition

Input Levels	GND to 3.0V
Transition Time	1.5 ns
Input and Output Signal Timing Reference Level	1.5 Volts
Ambient Temperature	0°C to 70°C
V_{CC}	3.3V ± 0.3V

Figure 3. AC Test Load Circuit (1)



Note: 1. Capacitive load consists of test environment.

Table 16. Read/Write AC Characteristics (T_A = 0 to 70 °C, V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	M63532P						Units
		-7		-8		-9		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{KC}	Cycle Time	13.3		15		16.7		ns
t_{KQ} (1)	Clock Access Time		7		8		9	ns
t_{OEQ} (1)	Output Enable Access Time		5		6		6	ns
t_{KQLZ} (2, 5)	Clock High to Q Active (Low-Z)	2		2		2		ns
t_{KQX} (1)	Clock High to Q Change	2		2		2		ns
t_{OELZ} (2, 5)	Output Enable to Output Active	0		0		0		ns
t_{KQHZ} (2, 5)	Clock High to Q High-Z		5		6		6	ns
t_{OEHZ} (2, 5)	Output Disable to Q High-Z		5		6		6	ns
t_{KH} (3)	Clock High Pulse Width	4.5		5.5		6		ns
t_{KL} (3)	Clock Low Pulse Width	4.5		5.5		6		ns
t_{AS} (4)	Address Set-up Time	2.5		2.5		2.5		ns
t_{ADSS} (4)	Address Status Set-up Time	2.5		2.5		2.5		ns
t_{DS} (4)	Data In Set-up Time	2.5		2.5		2.5		ns
t_{WS} (4)	Write/ Read Set-up Time	2.5		2.5		2.5		ns
t_{AAS} (4)	Address Advance Set-up Time	2.5		2.5		2.5		ns
t_{CES} (4)	Chip Enable Valid Set-up Time	2.5		2.5		2.5		ns
t_{AH} (4)	Address Hold Time	0.5		0.5		0.5		ns
t_{ADSH} (4)	Address Status Hold Time	0.5		0.5		0.5		ns
t_{DH} (4)	Data In Hold Time	0.5		0.5		0.5		ns
t_{WH} (4)	Write / Read Hold Time	0.5		0.5		0.5		ns
t_{AAH} (4)	Address Advance Hold Time	0.5		0.5		0.5		ns
t_{CEH} (4)	Chip Enable Hold Time	0.5		0.5		0.5		ns
t_{CFG} (6)	Configuration Set-up Time Prior to Device Operation	50		50		50		ns

Notes: 1. Measured with load as shown in Figure 3A.
2. Transition is measured ± 200mV from steady-state voltage with load as shown in Figure 3B. This parameter is sampled and not 100% tested.
3. This parameter is characterized and guaranteed and not 100% tested.
4. This is a synchronous device requiring that all inputs must meet the specified set-up and hold times with stable logic levels for all rising edges of the clock input (K).
5. At any given temperature or voltage condition, t_{KHQZ} is less than t_{KQLZ}, and t_{OEHZ} is less than t_{OELZ}.
6. Configuration signal $\overline{LBO}$ is static and must not change during normal operation.

Figure 4. Configuration Timing

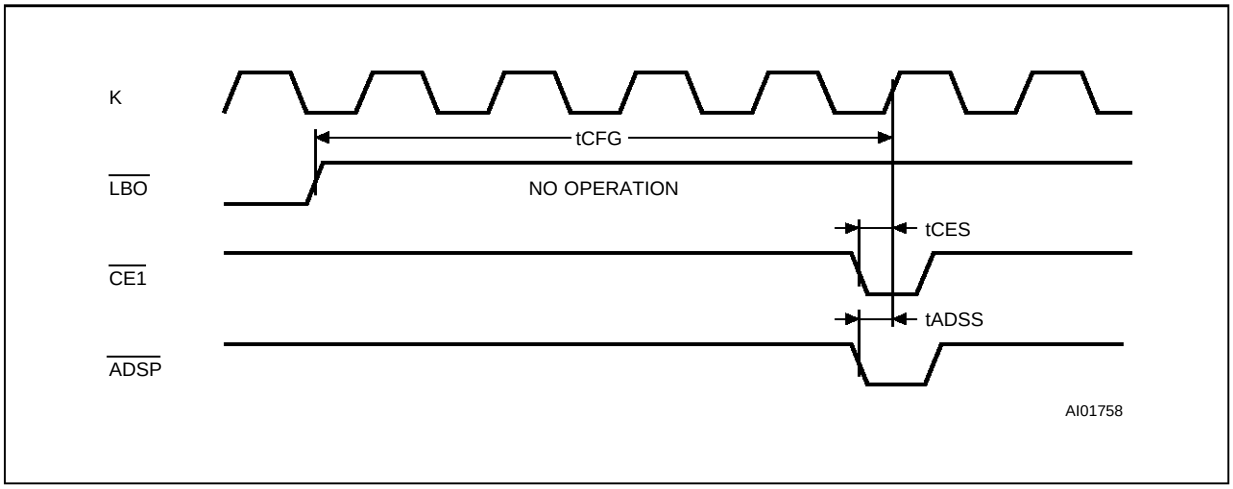


Figure 5. ZZ Mode Timing

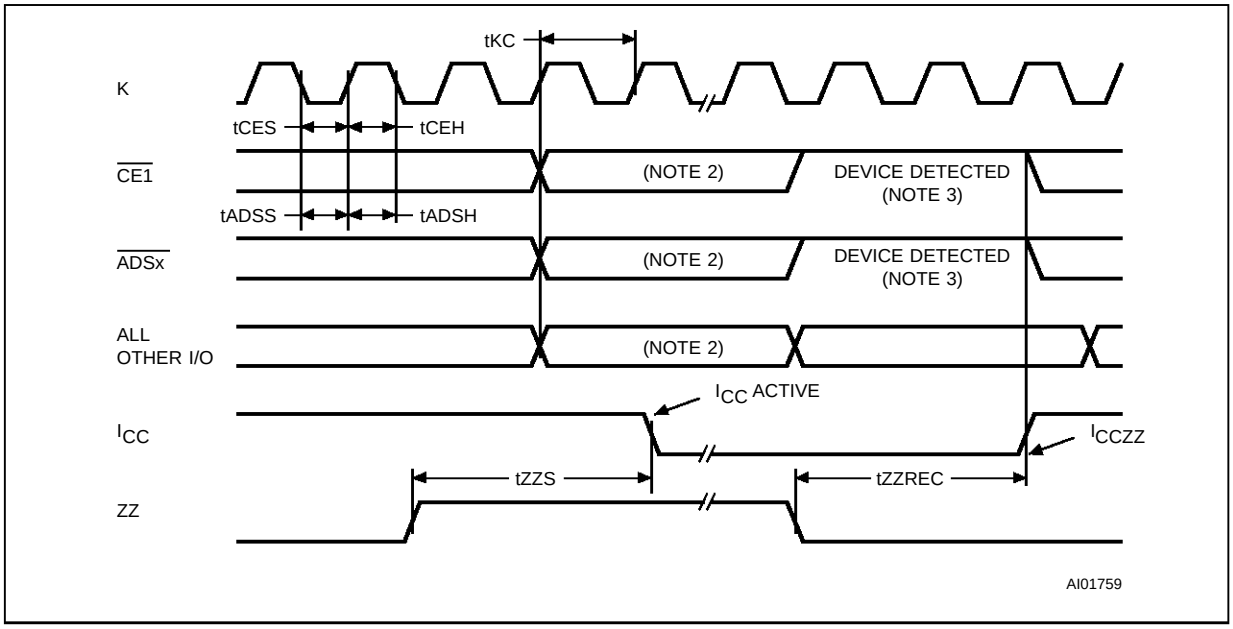
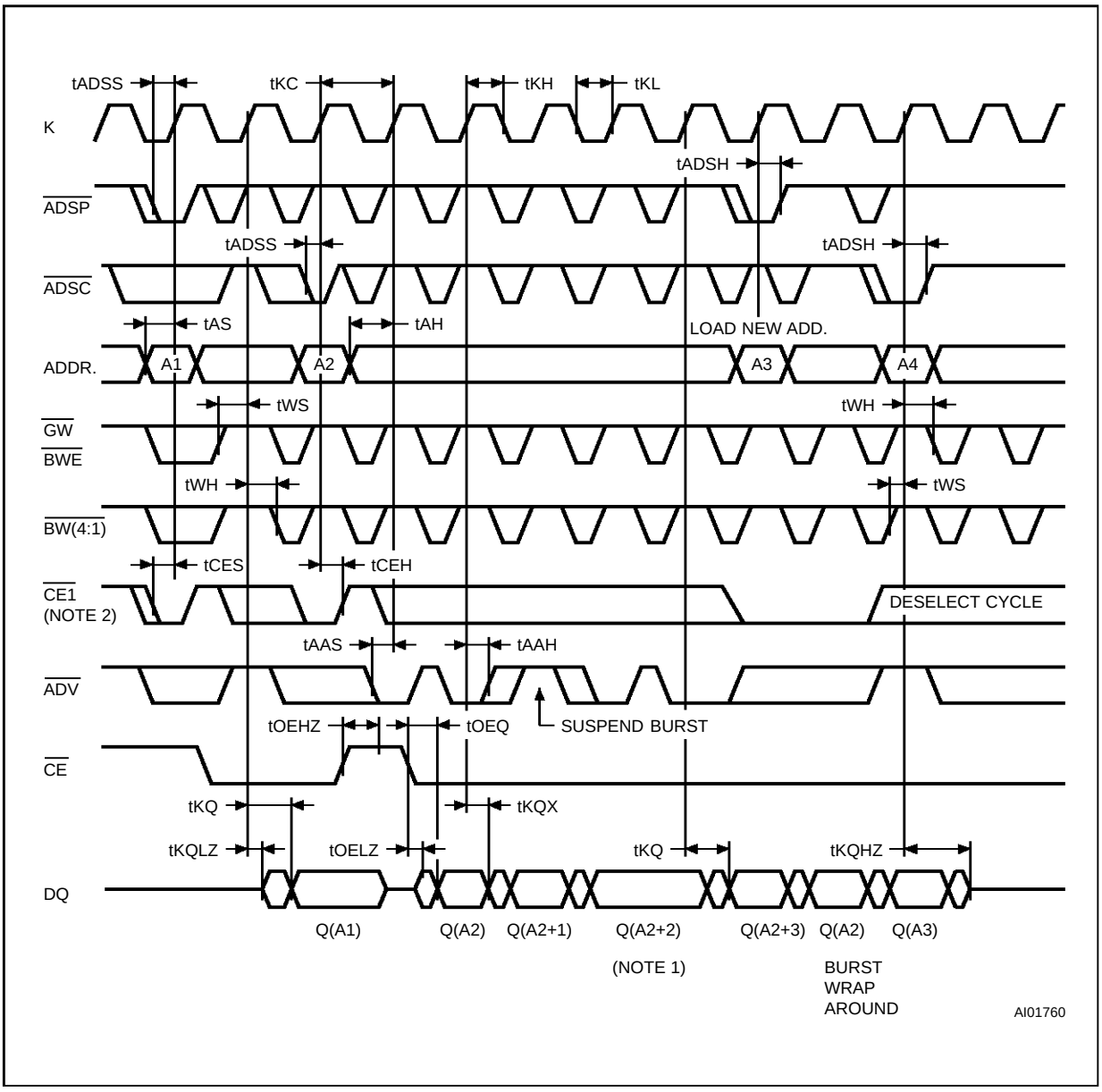


Table 17. ZZ Mode Data Retention Characteristics (1)
(T_A = 0 to 70 °C, V_{CC} = 3.3V ± 0.3V)

Symbol	Description	Conditions	Min	Max	Unit
I_{CCZZ} (2)	ZZ Mode Current	$V_{IN} \geq$ (Vcc –0.2V) or ≤ 0.2V; V_{CC} = 3.3V		2000	µA
t_{ZZS} (2)	Device Operation to ZZ StandbyTime	ZZ = HIGH $V_{IN} \geq (V_{CC}$ - 0.2V) or ≤ 0.2V; V_{CC} = 3.3V		$2t_{KC}$	ns
t_{ZZREC} (3)	ZZ Recovery Time	ZZ = LOW	$2t_{KC}$		ns

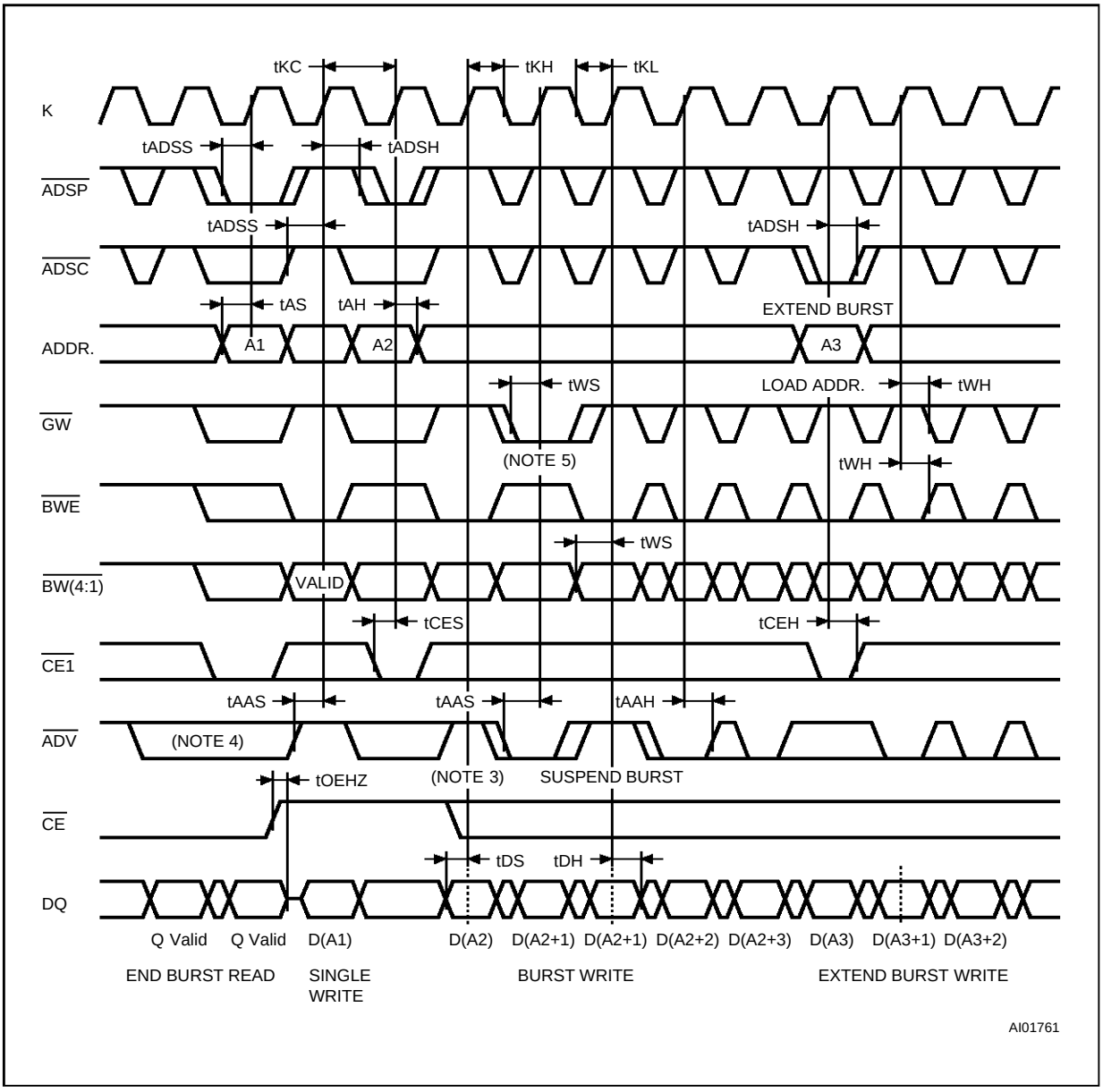
Notes: 1. The ZZ input pin is an asynchronous input asserted active HIGH. Any access pending when entering Snooze Mode is not considered valid, and completion of the operation is not guaranteed. Snooze Mode must not be initiated during a pending operation. It is suggested that the device be deselected before entering the Snooze Mode.
2. The assertion of ZZ allows the SRAM to enter a low power standby mode. Data integrity is guaranteed. All pins including the ZZ input = $V_{IN} \geq (V_{CC}$ –0.2V) or (GND ± 0.2V).
3. Chip Enables must remain False for the duration of t_{ZZREC} after the ZZ input returns LOW. Both $\overline{ADSP}$ and $\overline{ADSC}$ must remain HIGH during t_{ZZREC}.

Figure 6. Burst Read Cycle Timing (3)



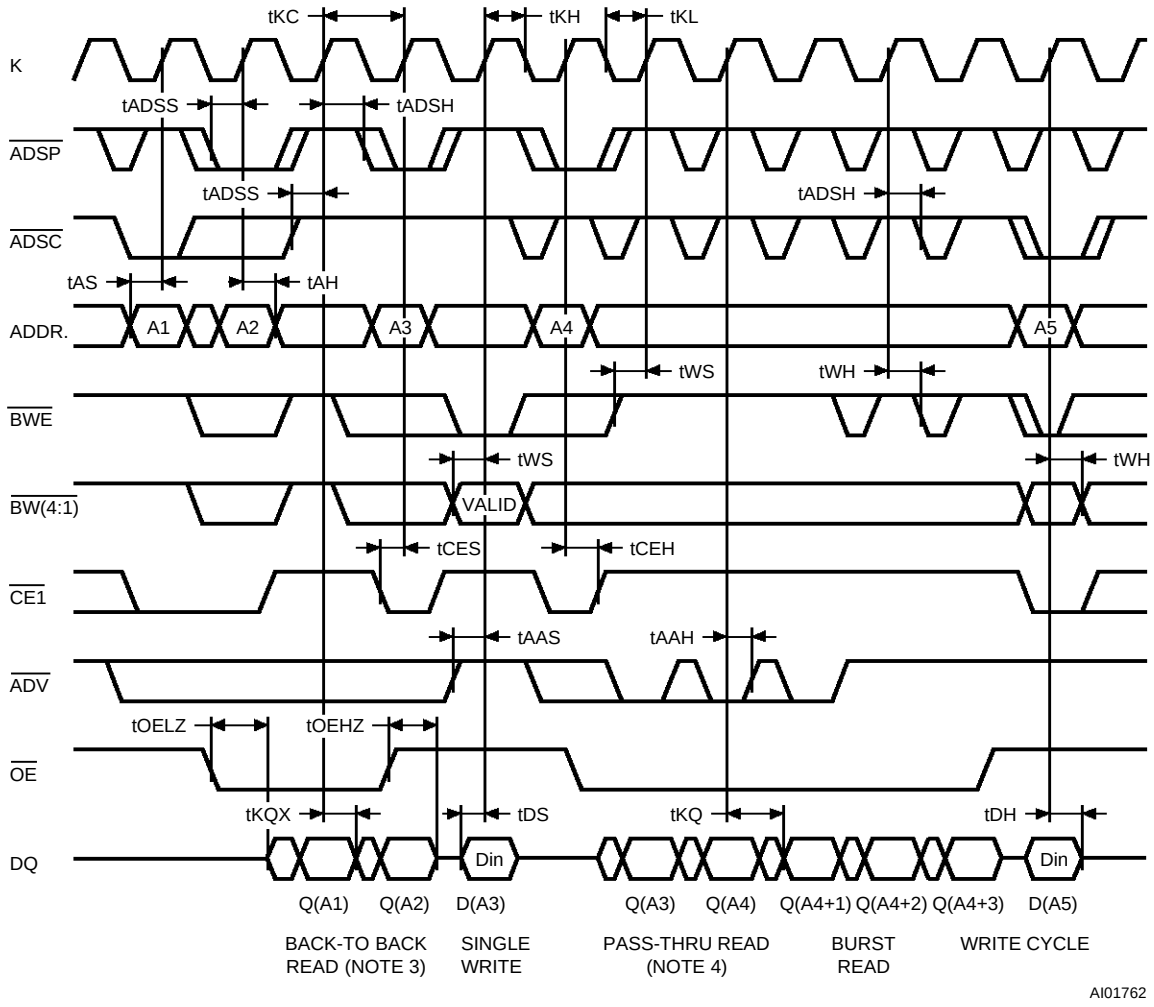
Notes: 1. Q (A2) represents the first output data from the base address A2. Q (A2+1) is the next output data in the burst read sequence with A2 as the base address. This is followed by subsequent bursts of output data Q(A2+2) and Q(A2+3) from base address A2.
2. In this diagram all Chip Enables have identical timing to $\overline{CE1}$. $\overline{CE1}$ and $\overline{CE3}$ are LOW while CE2 is HIGH. $\overline{CE1}$ and $\overline{CE3}$ are HIGH while CE2 is LOW.
3. This diagram shows the device as deselected at the beginning the timing sequence.

Figure 7. Burst Write Cycle Timing (1)



Notes: 1. D (A2) represents the first input data for the base address A2. D (A2+1) is the next input data in the burst write sequence with A2 as the base address. This is followed by subsequent bursts of input data D(A2+2) and D(A2+3) from base address A2.
2. In this diagram all Chip Enables have identical timing to $\overline{CE1}$. $\overline{CE1}$ and $\overline{CE3}$ are LOW while CE2 is HIGH. $\overline{CE1}$ and $\overline{CE3}$ are HIGH while CE2 is LOW.
3. $\overline{ADV}$ must be HIGH to permit a Write operation to the loaded address when using $\overline{ADSP}$ to load the external address.
4. $\overline{OE}$ must be HIGH prior to the input data set-up and held HIGH at least tDH. This prevents data bus contention.
5. All bytes are written when $\overline{GW}$ is sampled LOW ,or $\overline{GW}$ is HIGH and $\overline{BWE}$=BW1-BW4=LOW.

Figure 8. Combined Burst Read/Write Cycle Timing (2)



Notes: 1. In this diagram all Chip Enables have identical timing to $\overline{CE1}$. $\overline{CE1}$ and $\overline{CE3}$ are LOW while CE2 is HIGH. $\overline{CE1}$ and $\overline{CE3}$ are HIGH while CE2 is LOW.
2. $\overline{GW}$ is HIGH throughout this timing diagram.
3. Back-to-back Read cycles may be controlled by either $\overline{ADSP}$ or $\overline{ADSC}$.
4. Read pass-thru occurs when a Write cycle is followed by a subsequent Read cycle where the previously written data appears at the outputs in the same clock cycle that initiated the Read operation. $\overline{OE}$ controls the data bus at all times when the device is selected.

Figure 9. 256K Byte Cache Example

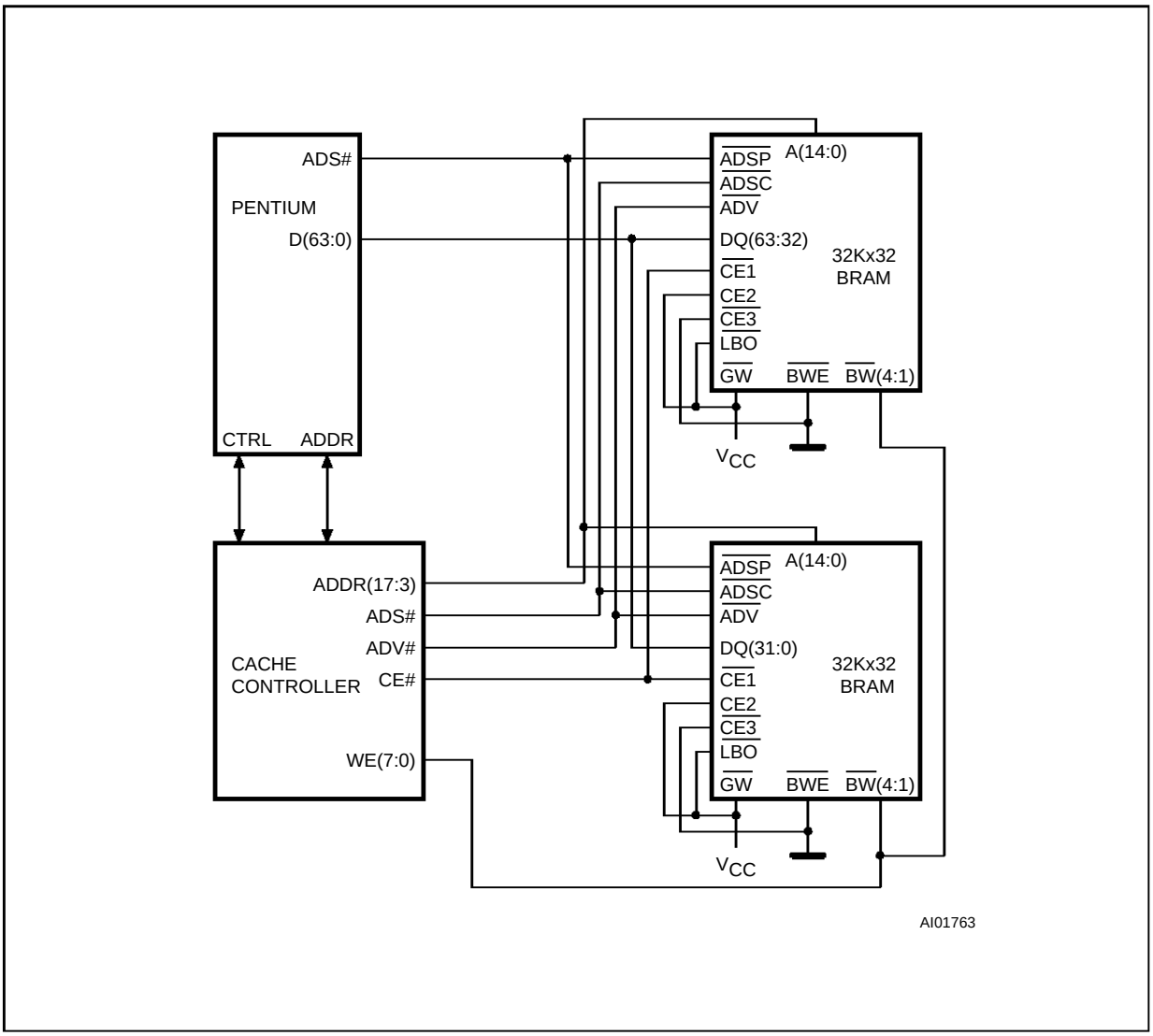
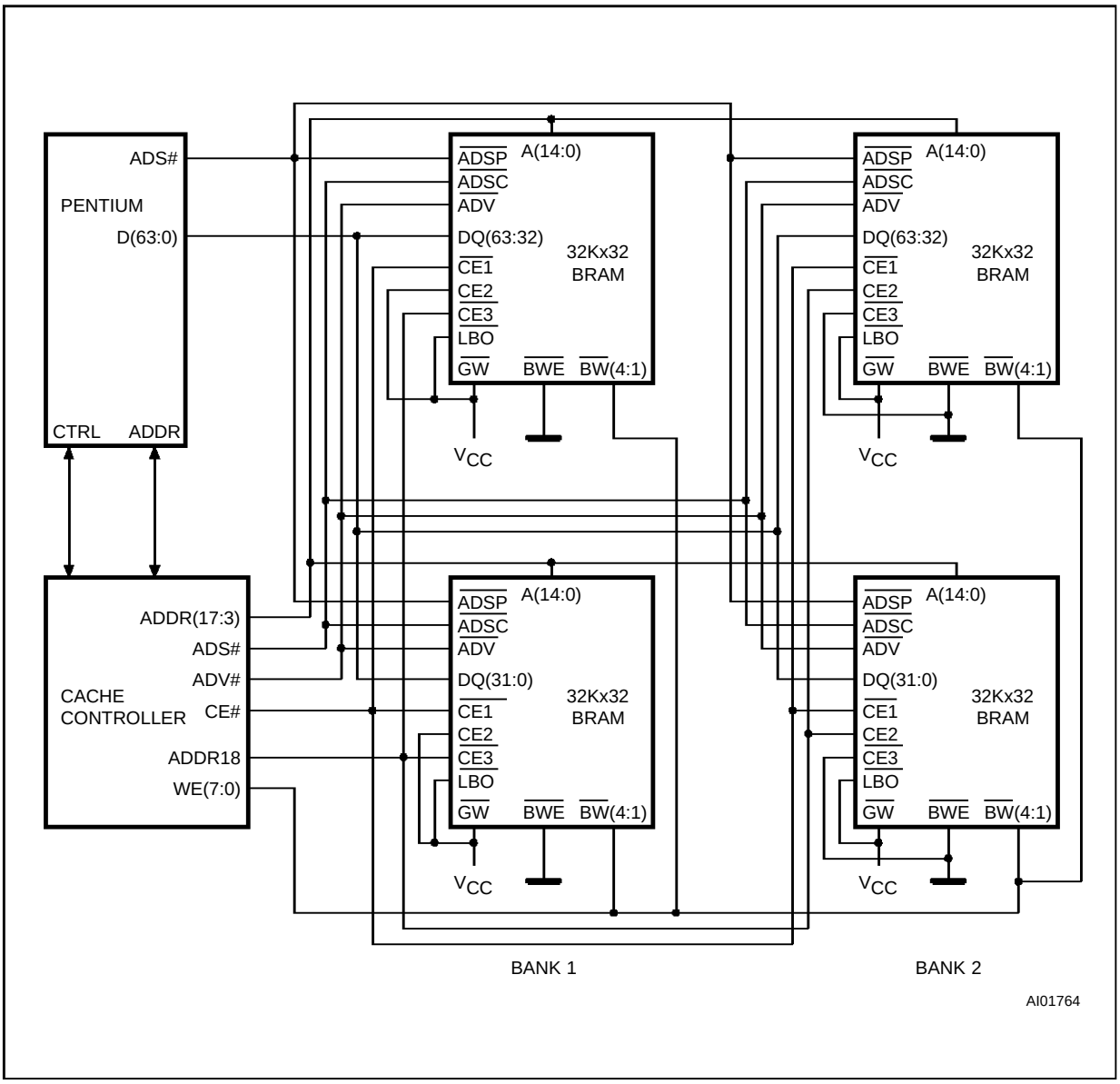
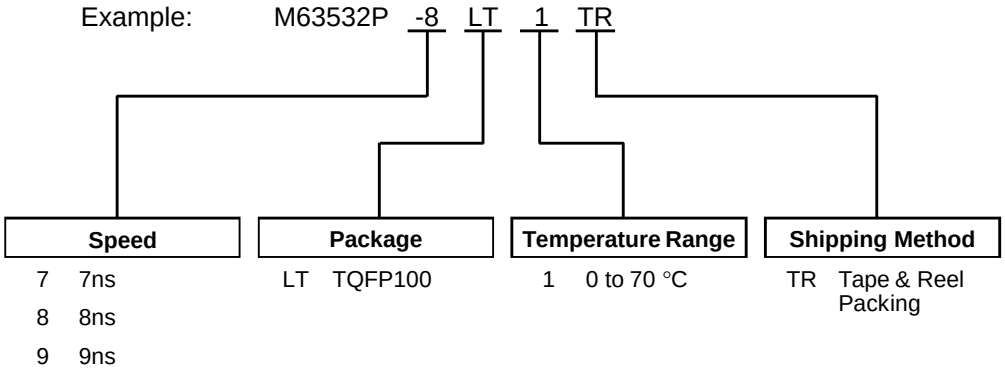


Figure 10. 512K Byte Cache Example



ORDERING INFORMATION SCHEME

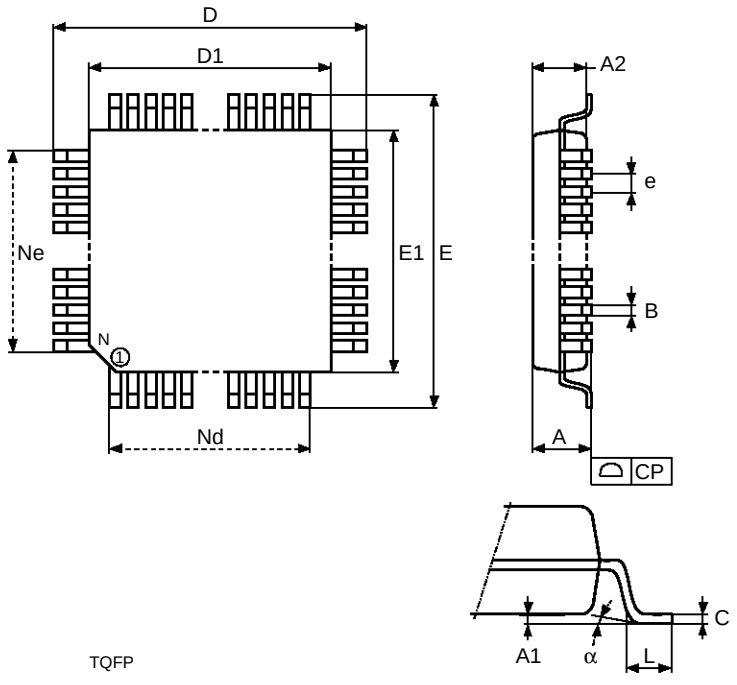


For a list of available options (Speed, Package, etc...) refer to the current Memory Shortform catalogue. For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

TQFP100 - 100 lead Plastic Thin Quad Flatpack, 14 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.40	1.60		0.055	0.063
A1		0.05	0.15		0.002	0.006
A2		1.35	1.45		0.053	0.057
B		0.22	0.38		0.009	0.015
C		0.15	0.19		0.006	0.007
D		21.90	22.10		0.862	0.870
D1		19.90	20.10		0.783	0.791
E		15.90	16.10		0.626	0.634
E1		13.90	14.10		0.547	0.555
e	0.65	–	–	0.026	–	–
L		0.45	0.75		0.018	0.030
α		0°	7°		0°	7°
N	100			100		
Nd	30			30		
Ne	20			20		
CP			0.10			0.004

TQFP100



TQFP

Drawing is not to scale